

Implementation of QCA XOR Gate Based on Interaction between QCA Cells

Jin-Seong Lee, Young-Won You and Jun-Cheol Jeon*

Abstract—Quantum-dot cellular automata (QCA) is an emerging technology for future computing. In this paper, we propose a new XOR gate based on QCA. The main building block of QCA circuit is majority gate and consequently the other logic circuits are implemented based on majority gate. On the other hand, our new XOR gate uses interaction between QCA cells. Main aim of the XOR gate has a low hardware complexity compared to previous design.

Keywords—Majority gate, Nanotechnology, XOR gate, Quantum-dot Cellular Automata.

I. INTRODUCTION

CMOS technology is reaching its physical limits while at the same time reliability and power issues are rising at alarming pace. In order to overcome these problems and to continue the trend of increasing integration densities, several new technologies have been proposed in recent years [1]. That said, CMOS does have many features that will cause both industry and academia to pursue scaling for the foreseeable future. The robustness of individual devices, relatively high fabrication yields, and existing infrastructure are just some of the characteristics that any new technology will need to eventually mimic. Additionally, with regard to interconnect, although wire delays and pitches may eventually limit scaling, the multiple layers of interconnect associated with CMOS have allowed designers to cross signals and wire up different parts of a circuit with relative ease. Although providing similar functionality has not been the most pressing focus for emerging nanoscale devices, many should still be able to promise at least one additional circuit "layer" for crossings (as efficient methods are essential to continue scaling at the system level). For example, systems of nanowires and nanotubes are orthogonal to each other and can leverage CMOS-like vias to cross signals [2].

Quantum-dot cellular automata (QCA) is one of the significant technology to be replaced with CMOS technology [3]. The unique feature is that logic states are not stored in voltage levels as in conventional electronics, but they are represented by a cell. A cell is a nano-scale device capable of encoding data by two-electron configuration. The cells must be aligned precisely at nano-scales to provide correct functionality, thus, the proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of

circuits [4], [5]. In this paper, we design a novel XOR gate based on interaction between QCA cells. The proposed circuits have been compared to previous circuit in number of cells, circuit complexity and clock phases.

II. RELATED WORKS

A. QCA Basic

A QCA structure is based on a cell which consists of four quantum dots, as shown in Fig. 1. The quantum dots are shown as the open circles which represent the confining electronic potential [6]. The electrons are allowed to jump between the individual quantum dots in a cell by the mechanism of quantum mechanical tunneling. Tunneling is possible on the nanometer scale when the electronic wavefunction sufficiently 'leaks' out of the confining potential of each dot, and the rate of these jumps may be controlled during fabrication by the physical separation between neighbouring dots [7]. Normally two electrons are placed diagonally. If cells are located like a Fig. 1(a), we call it a polarization of $P=+1$ and binary 1, while Fig. 1(b) are $P=-1$ and binary 0.

In QCA wires can be formed by arranging cells one after the other in line. In the wire signals propagate from the input to the output and the cells will assume polarization of the input signal [8]. There are two types of cell arrangement which shown in Fig. 2(a) and Fig. 2(b).

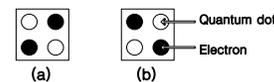


Fig. 1. QCA cell: (a) $P=+1$ (binary 1), (b) $P=-1$ (binary 0)

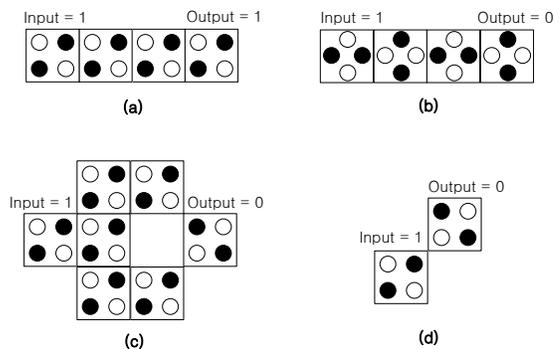


Fig. 2. QCA basic structures: (a) QCA wire, (b) Inverter chain, (c) Robust inverter and (d) Simple inverter

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J. S. Lee is with Kumoh National Institute of Technology, Gumi, KOREA.

*(Corresponding author) J. C. Jeon is with Kumoh National Institute of Technology, Gumi, KOREA.

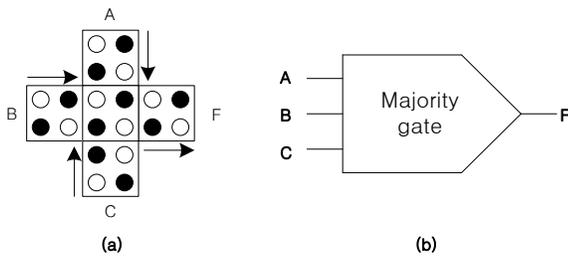


Fig. 3. QCA majority logic gate: (a) Using QCA cells, (b) Majority gate diagram

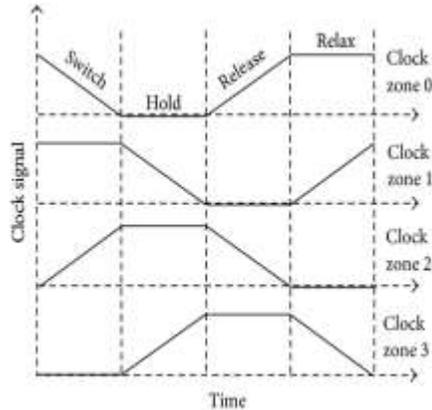


Fig. 4. QCA clock phases

Two standard cells in a diagonal orientation are geometrically similar to two rotated cells in a horizontal orientation. For this reason, standard cells in a diagonal orientation tend to align in opposite polarization directions as in the inverter chain. This anti-aligning behavior can be used in designing a QCA inverter [9]. Fig. 2(c) is a robust inverter and Fig. 2(d) is a simple inverter. A robust inverter is a stable state compared to simple inverter. A simple inverter is better than robust inverter in number of cells.

A majority gate is the basic block of QCA circuit. The QCA majority gate performs a three-input logic function. Assuming the inputs are A, B and C, the logic function of the majority gate is shown in (1) [10]. By setting one input permanently to logic '0' or logic '1', an AND gate or OR gate can be obtained. This result shown in (2) and (3). Fig. 3(a) show a QCA majority logic gate using QCA cell and Fig. 3(b) show a majority gate diagram.

$$M(A, B, C) = AB + BC + AC \quad (1)$$

$$M(A, B, 0) = AB + B(0) + A(0) = AB \quad (2)$$

$$M(A, B, 1) = AB + B(1) + A(1) = A + B \quad (3)$$

A series of QCA cells acts like a wire. During each clock cycle, half of the wire is active for signal propagation, while the other half is unpolarized. During the next clock cycle, half of the previous active clock zone is deactivated and the remaining active zone cells trigger the newly activated cells to be polarized. Thus, signals propagate from one clock zone to the next [11]. Each QCA cell is clocked using a four-phase clocking scheme as shown in Fig. 4.

B. XOR Gate

A XOR gate is a fundamental circuit to build the adder, comparator, parity generator and parity checker, due to the importance of XOR gate in digital logic system. Many XOR-based circuits have been proposed in QCA. The main building block of QCA circuit is majority gate and consequently the other logic circuits are implemented based on majority gate [12]. XOR gate is two input logic gate which output is 1, when two input operands are not same, the output is 0 otherwise. The functionality of XOR gate is shown in (4). Conventional block diagram of XOR gate consist of two AND gates and an OR gate.

$$F = AB' + A'B \quad (4)$$

III. PREVIOUS DESIGN

Previous XOR gates have been proposed in other papers [13], [14]. Angizi's XOR gate [13] uses a 5-input majority gate as shown in Fig. 5. This XOR gate consists of 67 cells and 5 clock phases. In [14], another XOR gate has been introduced as shown in Fig. 6. Mustafa's XOR gate uses a 3-input majority gates and 4 clock phases. The XOR gate consists of 41 cells, so that this structure has a low hardware structure and in comparison to the presented design in [16]. However, the input signal is located at inside of the circuit. It is not suitable to extend the other QCA circuits.

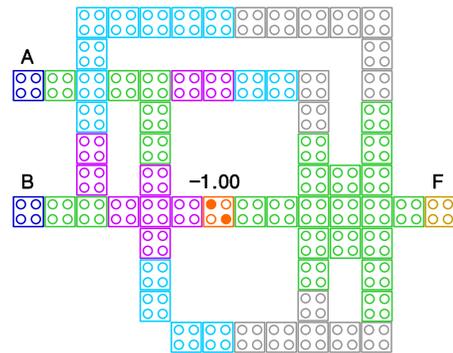


Fig. 5. Layout of previous XOR gate by Angizi [13]

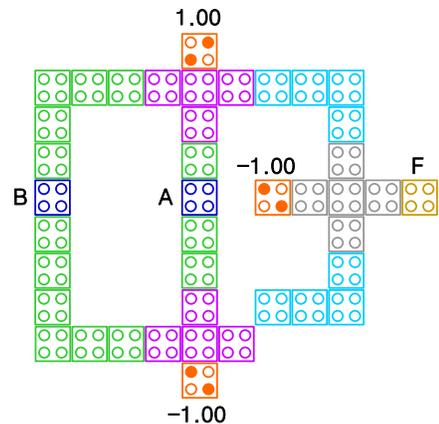


Fig. 6. Layout of previous XOR gate by Mustafa [14]

IV. PROPOSED DESIGN

In this paper, we propose a novel XOR gate based on interaction between QCA cells. Many XOR gates have been designed by majority gate. In order to low hardware complexity, we do not use any majority gate in our XOR gate. The design layout of XOR gate is shown in Fig. 8(a) and Fig. 8 (b) is simulation result of the proposed XOR gate. In Fig. 8(a), five cells of the inside of dotted line affect central cell and decide output state. Thus, we can reduce the number of cells, area and delay. It is consists of 10 cells and required only 2 clock phases. Block diagram of the XOR gate is shown in Fig. 7 and truth table of the XOR gate is shown in Table I.

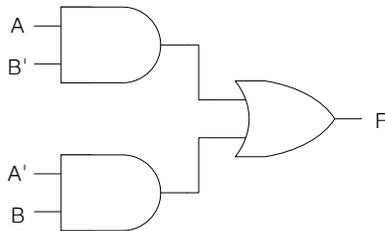
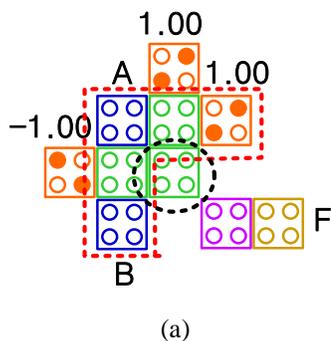


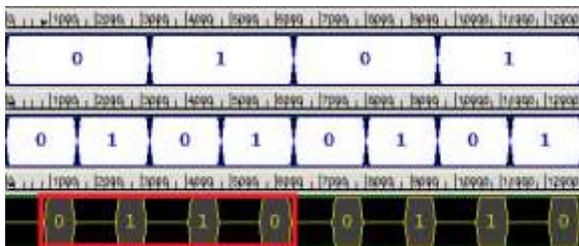
Fig. 7. Block diagram of XOR gate

TABLE I: TRUTH TABLE OF XOR GATE

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0



(a)



(b)

Fig. 8. Proposed XOR gate: (a) Layout of QCA, (b) Simulation result

V. COMPARISON AND ANALYSIS

The comparison of the number of cell, clock phase and used method are shown in Table II. In comparison, our XOR gate has 85.1%, 75.6% improvement in the number of cells compared to previous designs. Also, we have low clock phases as compared to previous structures. The previous designs have been proposed based on majority gate, but our XOR gate used interaction of QCA cells.

TABLE II: COMPARISON OF XOR GATE

	Angizi et al. [13]	Mustafa et al. [14]	Ours
Number of cell	67	41	10
Clock phase	5	4	2
Used method	Majority	Majority	Cells interaction

VI. CONCLUSION

In this paper, a novel XOR gate has been proposed with low hardware complexity and high speed in computation. The XOR gate designed based on interaction between QCA cells. Hence, our structure is advanced more than previous design in number of cells and clock phases.

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Jin-Seong Lee, He received B.S. in applied mathematics from Kumoh National Institute of Technology, Korea in 2016. Currently, he is doing M.S. in computer engineering at Kumoh National Institute of Technology, Korea. His major research interests are in quantum cryptography and quantum cellular automata.



Young-Won You, He is doing B.S. in computer engineering at Kumoh National Institute of Technology in 2016. His current research interests are in quantum cryptography and quantum-dot cellular automata.



Jun-Cheol Jeon, He is currently a professor in Department of Computer Engineering at Kumoh National Institute of Technology. He received B.S. degree from Kumoh National Institute of Technology in 2000, the M.S. and Ph.D. degrees from Kyungpook National University in 2003 and 2007 respectively. His current research interests are cryptography, cellular automata, quantum-dot cellular automata and quantum computation.