Full Adder Based on Quantum-dot Cellular Automata

Nuriddin Safoev and Jun-Cheol Jeon*

***Abstract*—The full adder is a basic combinational building in any arithmetic circuits and great deals of attention have been paid for this research field. In this paper an improved QCA full adder is proposed. It is considerably declined in terms of hardware complexity, such as cell numbers, delay and total area aspects compared to other existing full adders. The simulation results of presented full adder in QCADesigner tool confirm that the proposed circuit works well and it can be used as a high performance design in arithmetic circuits.**

***Keywords*— Full adder, Nanotechnology, Quantum-dot cellular automata, QCA cell.**

I. INTRODUCTION

QCA is the computing with cellular automata composed of arrays of quantum-dot devices, and basic concepts were introduced by Tougaw and Lent in 1993[1]. The unique feature is that logic states are not stored in voltage levels as in conventional electronics, but they are represented by a cell. A cell is a nano –scale device capable of encoding data by two-electron configuration. The cells must be aligned precisely at nano-scales to provide correct functionality, thus, the proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of circuits [2]. Transmission of the data in QCA is realized using clocking technique. It is controlled by a tunneling barrier. According to the moving up or down of the tunneling barrier, the clocking technique consists of four stages: locking locked, relaxing and relaxed [3, 4].

QCA has several advantages over CMOS technology. Some of the advantages include faster switching speeds, high density circuits and low power consumption. The assumption is that all these advantages will bring highly result in the development of powerful and efficient computers [4, 5].

Full adder is one of the most frequently used components in arithmetic units. Actually, function of full adder is addition and also it is utilized as a core part in other arithmetic operations like subtraction, division and multiplication. In this case, designing efficient QCA full adder is a great solution to increase developing process of QCA arithmetic circuit aspects [6].

This paper introduces less hardware complexity full adder using three input exclusive OR gate(TIEO) which was proposed by Ahmad et al. It can be easy to extend serial adder as ripple carry adder. Using this approach provides improved area and delay to other recent design.

This paper is organized as follows. In section 2, we have provided with information about basic concept of QCA technology and next stage one-bit QCA full adder. In section 3, we have proposed our full adder and have demonstrated simulation results. Collected information which is according to previous section, we have compared and analyzed in section 4. Finally, we have concluded the paper in section 5.

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II. RELATED WORKS

A. QCA Basic

The basic building block of QCA is a cell and it is constructed from four quantum dots. A high-level diagram of two polarized QCA cells is shown in Figure 1. Each cell is constructed from four quantum dots arranged in a square pattern. The cell is charged with two electrons, which are free to tunnel between adjacent dots. These two arrangements are denoted as cell polarization P = +1 and P = -1 respectively. By using cell polarization P = +1 to represent logic "1" and P = -1 to represent logic "0", binary information can be encoded [7, 8].

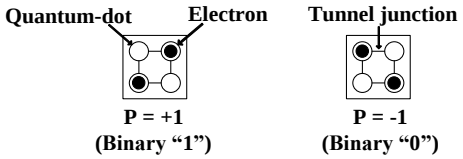

Fig. 1. Basic QCA cells with two polarizations.

By placing QCA cells side-by side, a QCA standard wire is constructed. In a QCA wire, the binary signal propagates from input to output because of the coulombic interactions between cells. The wire can be formed by placing cells one after another one as a shown in Figure 2(a). In the information propagation process, if the input is one, then the signal transferred from input to the output will be one or if the input is zero, then zero transferred to the output.

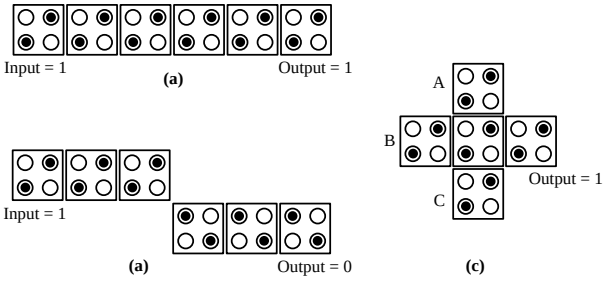

Fig. 2. QCA basics: (a) standard wire, (b) inverter, (c) 3-input majority gate.

Any QCA circuit can be efficiently built using QCA fundamental structures. In most of circuits, inverter and majority gates are used to design. As illustrated in Figure 2(b), the input polarization is inversed when the signal reaches the output cell. This kind of inverter is two-cell-inverter. Majority gates play significant role in conventional circuit design. In this case, complexity of the structure has been relatively associated to the cell configuration of QCA fundamental gates. Figure 2(c) shows the structure of the majority gate and it consist of three input cells, one inside cell and one output cell. The logic function of a majority gate is shown in Equation 1.

$$M(A,B,C) = AB + BC + AC \quad (1)$$

General terms an AND and OR gates will be obtained by fixing polarization one input of the majority gates. All logical function can be implemented using combination of inverter and majority gates.

B. *Clocking in QCA*

Clocking in QCA leads to adjustment of tunneling barriers between quantum dots for transfer of electrons between the dots. QCA clocking controls information flow and provides with power to run the circuit. Figure 3 shows clocking of a QCA cell. It consists of four phases: switch, hold, release and relax. The phases of clock change, when the potential barriers are raised or lowered [5, 9].

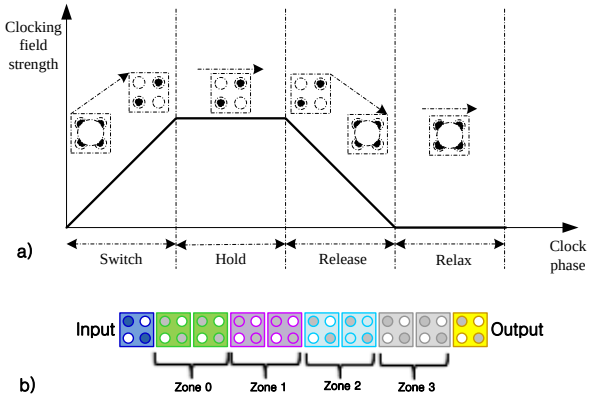

Fig. 3. Concept of QCA clocking: (a)clock zone of wire, (b)four phases switching wire in QCA

In the switch phase, the inter-dot barrier is gradually raised and the cell settles down to one of the two ground polarization states. High inter dot barrier is held in the hold phase. During the release and relax phases, the inter dot barriers are comparatively low and the excess electrons gain movement. In these two phases QCA cell remains unpolarized.

C. *Wire crossing in QCA*

Some issue occurs with wire crossing in QCA circuit design. Basically, there are two types of wire crossing namely multilayer and coplanar crossing technique. Tougaw and Lent [10] proposed a coplanar crossover as shown in Figure 4(a). In this method, vertical and horizontal wires transmit the value one and zero, respectively.

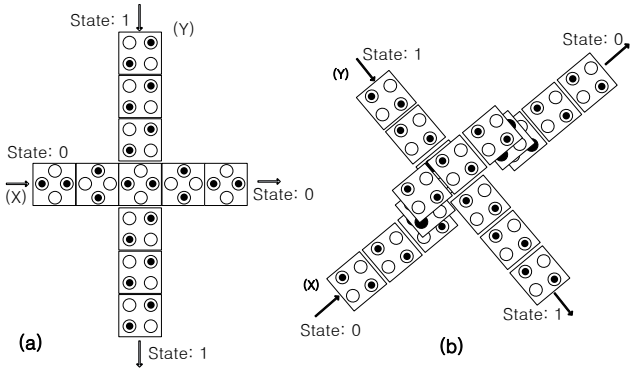

Fig. 4. Wire crossing in QCA: (a)coplanar crossover, (b)multilayer crossover.

Implementation of this wire crossing is based on rotated QCA cell, namely cells of horizontal wire are rotated by 45°. The number of cells in the horizontal wire should be composed of odd because of the characteristic of rotated cells [11].

The stability of coplanar crossover is less compared to the multilayer crossover. On the other hand, it is difficult to fabricate multilayer crossover. QCA regular cells are used in our paper, for this reason, multilayer crossover is utilized in this design and also we need more stable signal for our design.

D. *QCA full adder*

An adder is a digital circuit that performs addition operation. Other kind of operations such as subtraction, division and also multiplication are usually constructed using adders. A full adder adds three one-bit numbers. It has a three-input (A, B, Cin) and two-output (Carry and Sum) building blocks.

We review various schematic equations of one-bit full adders which have been presented in other papers. The first proposed formulation was presented in equation(2). However, its QCA clocking concept was not considered [12]. It consists of five majority gate and three inverters. Majority based carry formula has been achieved significantly as shown below.

$$Carry = MG(A,B,Cin); \quad (2)$$
$$Sum = M\left(M\left(A,\overline{B},Cin\right),M\left(A,B,\overline{Cin}\right),M\left(\overline{A},B,Cin\right)\right)$$

Hence, other formulation proposed for Sum. A modification of the first sum was proposed by [13] with clocking concept. It has four majority gates and three inverters.

Equation(3) is another formula for sum and it has three majority gates and two inverters with five clocking phase.

$$Sum = M\left(\overline{Carry}, M\left(A,B,\overline{Cin}\right), Cin\right) \quad (3)$$

After proposed various five input majority gates, new formulation for sum is presented by researchers [14].

$$Sum = M\left(\overline{Carry}, \overline{Carry}, A, B, Cin\right); \quad (4)$$

It gives significant effect for hardware complexity. In this case, the most QCA full adders implemented based on this equation.

Our proposing design for full adder depends on gate state three-input exclusive OR gate which was introduced in [15]. Its concept is similar with single layer five input majority gate

[14]. Designs of gate are presented in Figure 5.

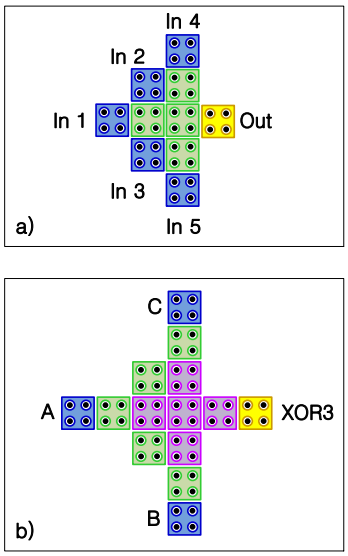

Fig. 5. (a) 5-input majority gate, (b) explicit interaction 3-input XOR(TIEO).

Implementation of three input XOR gate is constructed with explicit interactions between QCA cells. The gate consists of only 14 cells with 0.5 clock cycles. By fixing one of the inputs in Figure 5(b), namely input A to the binary 0, simple two input XOR gate can be constructed.

The proposed design in [15] can be effectively converted to a three-input XOR gate with similar latency, cell count and area to those of its two input implementation. The presented design has achieved significant improvements in terms of hardware complexity, latency and with other aspects.

Less wire crossing in QCA circuit is the most important gain. In one bit QCA adder, the sum can be achieved with 3-input XOR gate. Hence, to use the sum bit of the full adder as QCA gate condition can bring good solution for complex structures.

III. Proposed QCA Full Adder

In this section, we are going to present one bit full adder. Logical block diagram of the structure has been presented in Figure 6. The implementation of full adder is constructed by two gates in three layers. In the main layer carry bit is formed by conventional three input majority gate. In the upper layer we have used three-input XOR (TIEO) gate which is shown in Figure 5(b).

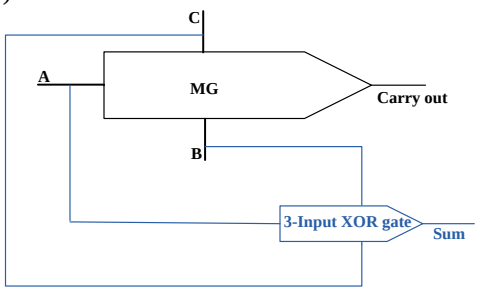

Fig. 6. Logical diagram of proposed full adder.

Proposed QCA one bit full adder has 31 standard cells and 0.5 clock latency. Coherence vector and bistable approximation engines of QCADesigner tool version 2.0.3 [16] are used to verify circuit functional behavior. The designer tool illustrates that simulation waveform in Figure 8 has shown correctly result.

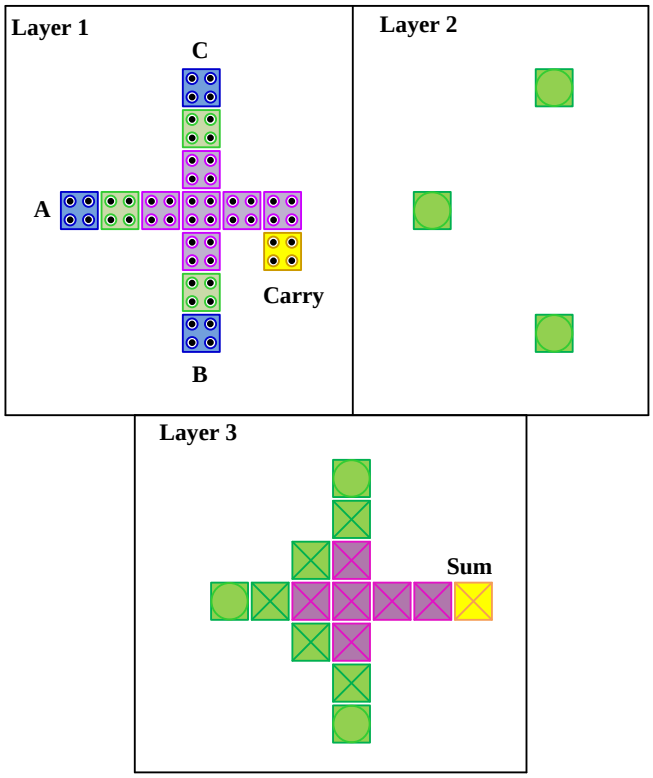

Fig. 7. Construction of proposed full adder.

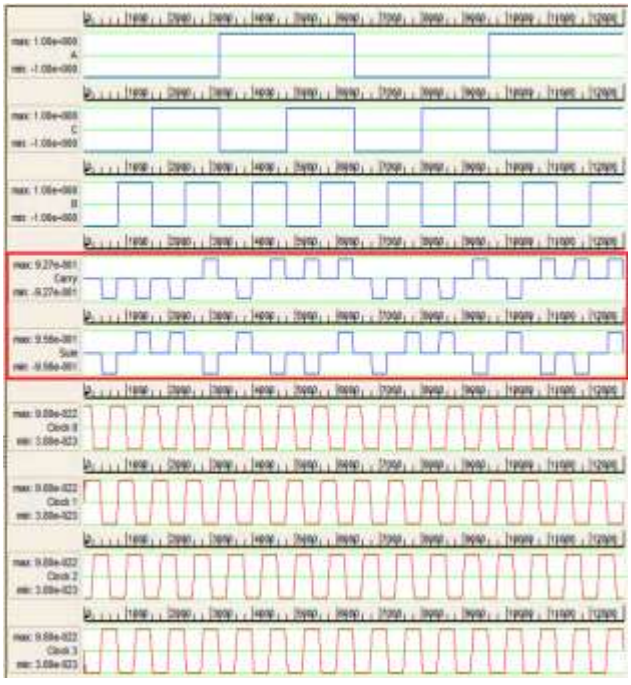

Fig. 8. Simulation waveform of proposed full adder.

IV. Comparison and Analysis

The performance of proposed full adder has been compared with other existing adders in three metrics as shown in Table 1

and. It may be noted that usually, multilayer designs are expected to consume much smaller are than their coplanar ones. In our proposed design, the multilayer crossover is used to get high performance. Actually, multilayer crossover is not used for crossing wire, it is just used for construction full adder as intact. Speed of QCA circuit is measured using latency and also it is considered the important metric of the circuit. The proposed adder performs fairly well. Its clocking phase is realized fast. As is shown, our proposed design uses 31 cells, two clock phase and approximately 0.015 μm^2 area. It can be clearly seen that proposed adder performs fairly well as compared to existing adders.

TABLE I: STRUCTURAL ANALYSIS OF FULL ADDERS

Circuit	Cell count	Total area	Delay
In Ref. [5]	145	0.17	5
In Ref. [14]	73	0.04	3
In Ref. [17]	61	0.03	3
In Ref. [18]	51	0.03	3
In Ref. [19]	38	0.02	3
Proposed design	31	0.02	2

V. CONCLUSION

In this paper, less hardware complexity QCA full adder is presented. It has achieved significant improvements in the terms of cell numbers, area and latency. In addition construction method is also simple to extend to large bit adders. Because the structure consists of two gates, namely three-input majority gate and three input XOR gate(TIEO)[15]. In the comparison, our proposed full adder has better performance.

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